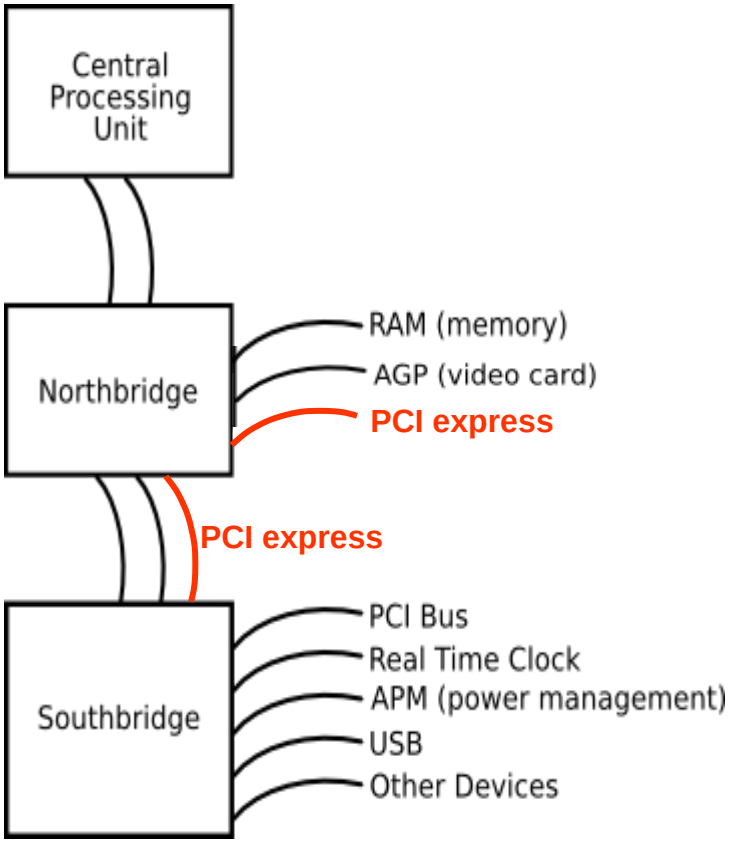
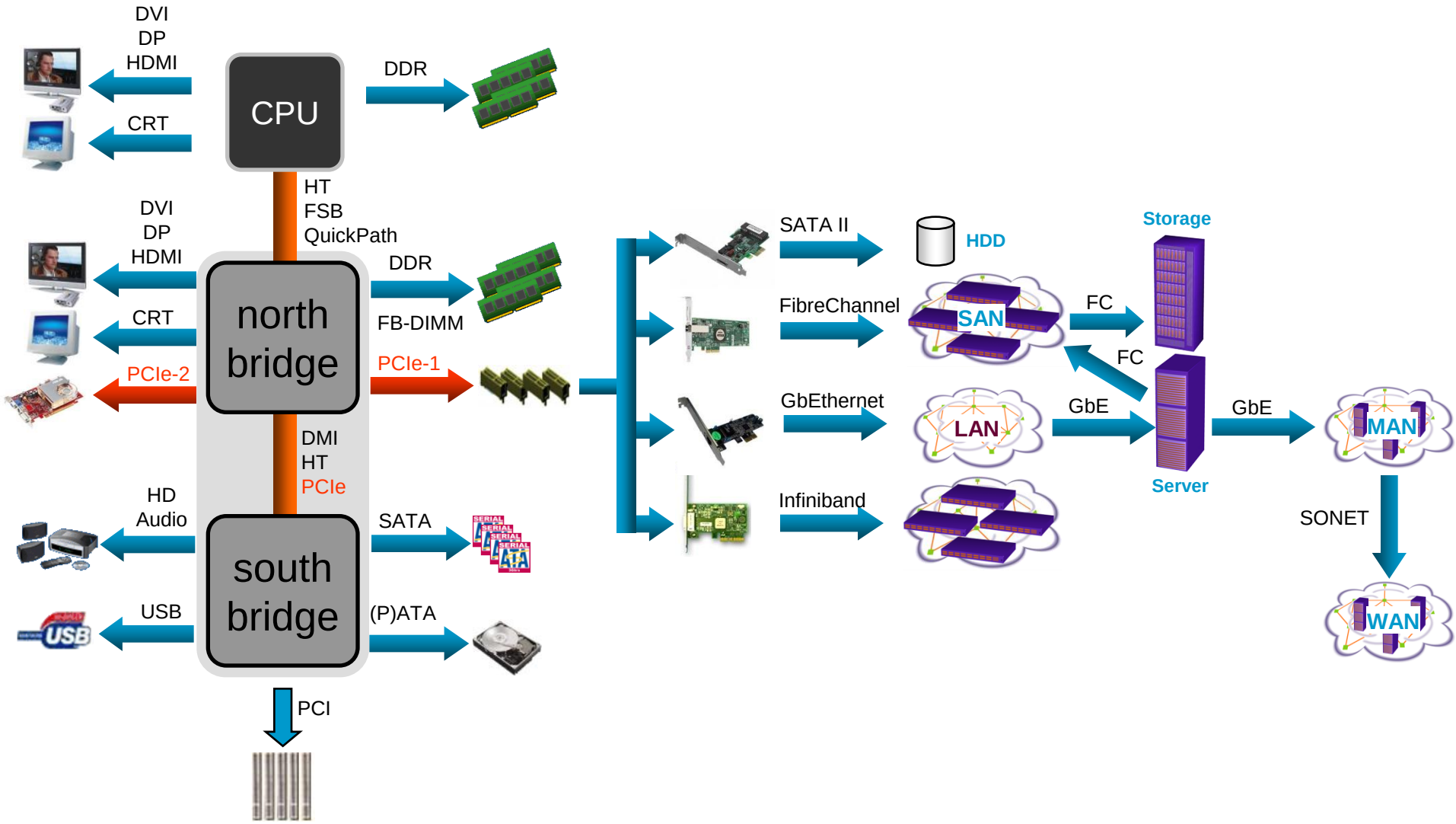
PCI Express®

- PCI Express : Where is it used in computers?
- DUTs and J-BERT match
- Testing PCI Express
  - PCIe 2 theory
  - realization of RX-tests w/ J-BERT-A
- PCIe 3, another outlook

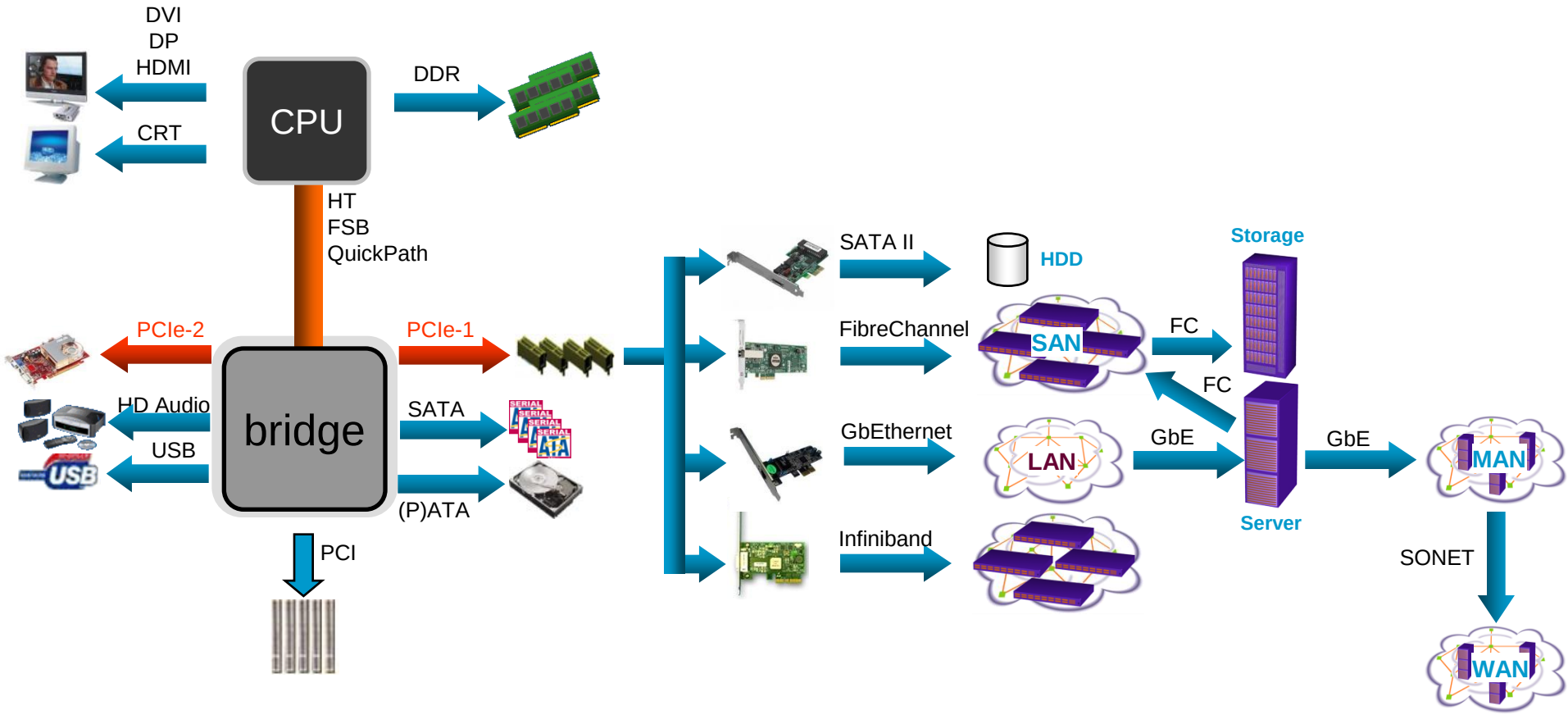
Processor Architecture Block Diagram for PCIe



Processor Architecture Block Diagram for PCIe



Processor Architecture Block Diagram for PCIe



Testing PCI Express Electrical Layer

PCI Express Electrical Layer Test

Physical Layer Measurements

TX waveform characterization and jitter decomposition

Infiniium Scope

Jitter transfer PLL or CDR frequency response measurements

RX sensitivity and jitter tolerance test

J-BERT

DUTs and Tests

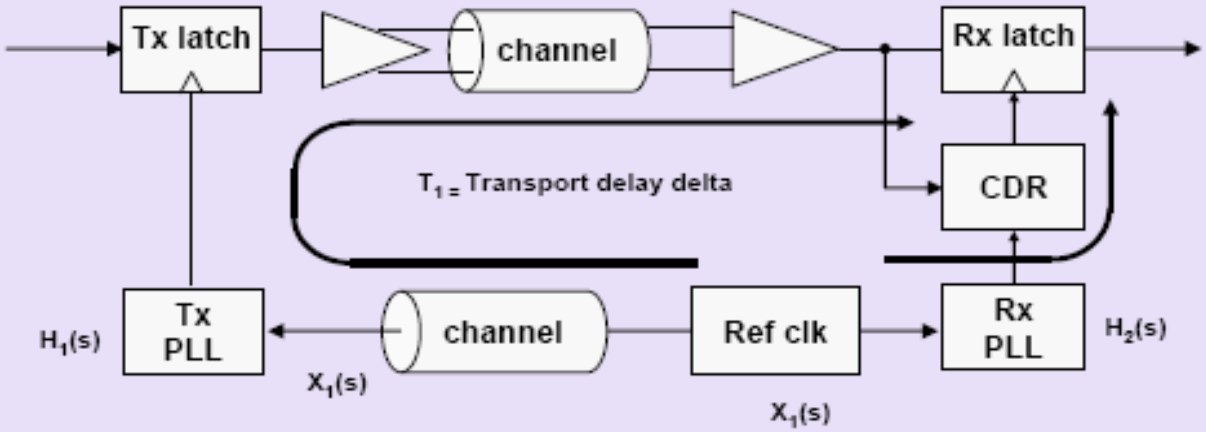
DUT	**mandatory test /** ***recommended tests***	**relevant spec**
I/Os of test chips	TX, RX, jitter transfer	PCIe base spec
I/Os of final ASICs		
Add in cards (graphic)	TX, jitter transfer	CEM card spec
Motherboards	*RX sensitivity w/ stressed eye*	

Which Tests, Addressed When and How

Test	Now
RX sensitivity and jitter tolerance	J-BERT A + 81150A & 15431A for correct RJ spectrum trace #2 for ISI / DJ
TX waveform tests	Scope
TX jitter transfer	Scope

The Theory Behind the Specs

Common Clock Topology



$$H(s)=\left[\underbrace{\frac{2s\zeta_1\omega_{n1}+\omega_{n1}^2}{s^2+2s\zeta_1\omega_{n1}+\omega_{n1}^2}}_{\text{5 MHz, 1 dB or 8 MHz, 3 dB}}e^{-sT_1}-\underbrace{\frac{2s\zeta_2\omega_{n2}+\omega_{n2}^2}{s^2+2s\zeta_2\omega_{n2}+\omega_{n2}^2}}_{\text{16 MHz, 3 dB}}\right]$$

$$Y(s)=X_1(s)*H(s)$$

PLL difference function

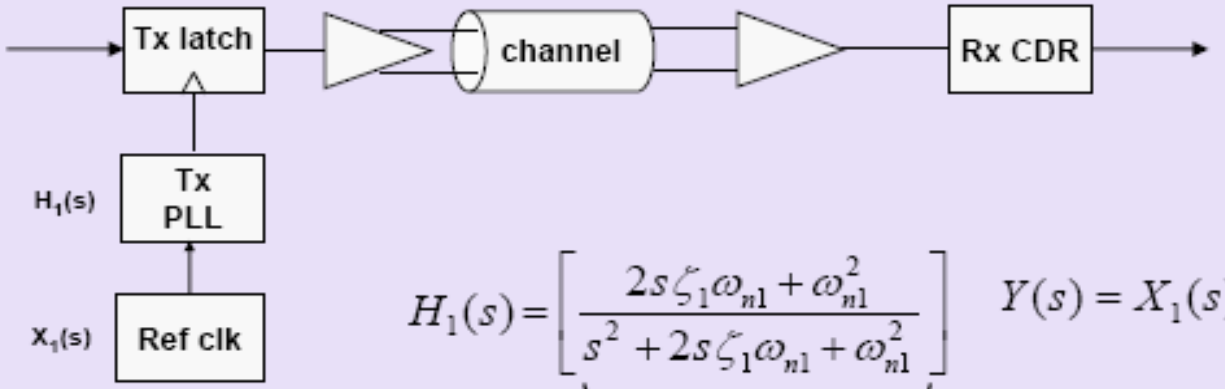
- **Tx and Rx paths track LF jitter in accordance with PLL difference function.**
- **PLL difference function removes jitter in below 5 MHz and above 16 MHz**
- **SSC residual jitter reduced to 33 KHz, 75 ps triangular waveform**

5.0 GT/s Rx Tolerancing Parameters (common clock architecture)

Parameter	Description	Min	Max	Units
UI	Unit Interval	199.94	200.06	ps
$T_{RX\_HF\_RMS}$	> 1.5 MHz Rj		3.4[1]	ps RMS
$T_{RX\_HF\_DJ\_DD}$	> 1.5 MHz Dj (including channel effects)		88[2,3]	ps
$T_{RX\_SSC\_RES}$	0-1.5 MHz Dj (SSC residual)		75[4]	ps
$T_{RX\_LF\_RMS}$	0-1.5 MHz Rj		4.2	ps RMS
$T_{RX\_MIN\_PULSE}$	Minimum width pulse at Rx	120		ps
$V_{RX\_MAX\_MIN\_RATIO}$	min/max pulse voltage ratio on consecutive UI		5	--
V_{RX_EYE}	Receive eye voltage aperture	120	1200	mV
$V_{RX\text{-}CM\text{-}AC\text{-}PP}$	Common mode noise		300	mVPP

1. Jitter BW: 1.5 – 100 MHz, spectrally flat, consisting of contributions from Refclk and Tx
2. Includes sinusoidal component plus channel effects. Sinusoid swept continuously from 1.5 – 100 MHz or over same range in 10^{th} octave steps
3. Two different tests must be performed: maximum channel with minimum sinusoidal Dj and zero channel with max sinusoidal Dj. In both cases Dj total = 88 ps pp.
4. SSC residual consists of 33 KHz triangular wave with 75 ps PP magnitude
5. 0 – 1.5 MHz, spectrally flat, consisting of contributions from Refclk and Tx

Data Driven Topology



$$H_1(s) = \underbrace{\left[\frac{2s\zeta_1\omega_{n1} + \omega_{n1}^2}{s^2 + 2s\zeta_1\omega_{n1} + \omega_{n1}^2} \right]}_{\text{16 MHz, 3 dB}}$$

$$Y(s) = X_1(s) * H_1(s)$$

PLL difference function

- The full 20 ns of SSC jitter must be tracked by the CDR
- Receiver must track additional <1.5 MHz Rj and Rj in the 1.5-8 MHz range that would otherwise be removed by the PLL difference function in the CC case.
- Rx must also track LF Refclk jitter from 1.5 MHz down to 10 KHz

5.0 GT/s Rx Tolerancing Parameters (data driving architecture)

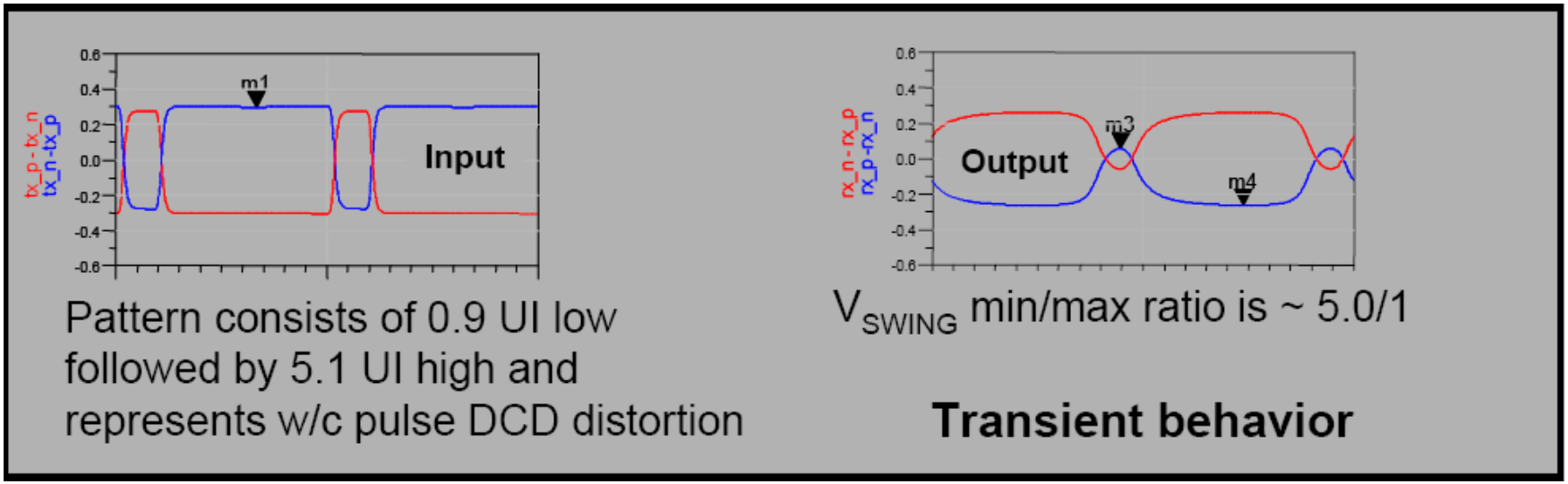
Parameter	Description	Min	Max	Units
UI	Unit Interval	199.94	200.06	ps
$T_{RX\_HF\_RMS}$	> 1.5 MHz Rj		4.2[1]	ps RMS
$T_{RX\_HF\_DJ-DD}$	Max Dj impinging on Rx under tolerancing		88[2,3]	ps
$T_{RX\_LF\_SSC\_FULL}$	0-1.5 MHz Dj (Full SSC)		20[4]	ns
$T_{RX-LF-RMS}$	10 Khz – 1.5 MHz RMS jitter		8	ps RMS
$T_{RX\_MIN\_PULSE}$	Minimum width pulse at Rx	120		ps
$V_{RX\_MAX\_MIN\_RATIO}$	min/max pulse voltage ratio on consecutive UI		5	--
V_{RX_EYE}	Receive eye voltage aperture	100		mV
$V_{RX-CM-AC-PP}$	Common mode noise		300	mVPP

1. Spectrally flat from 0 – 1.5 MHz. Includes 3.9 ps from Refclk and 1.4 ps from Tx
2. Two different tests must be performed: maximum channel with minimum sinusoidal Dj and zero channel with max sinusoidal Dj
3. Two different tests must be performed: maximum channel with minimum sinusoidal Dj and zero channel with max sinusoidal Dj
4. Full SSC must be tracked. Includes sinusoidal component plus channel effects.
5. Over 10 KHz – 1.5 MHz BW with -20 dB/decade to account for 1/f noise slope

RX Jitter Tolerance Specs
Based Upon Channel Behavior: DJ (ISI+PJ)

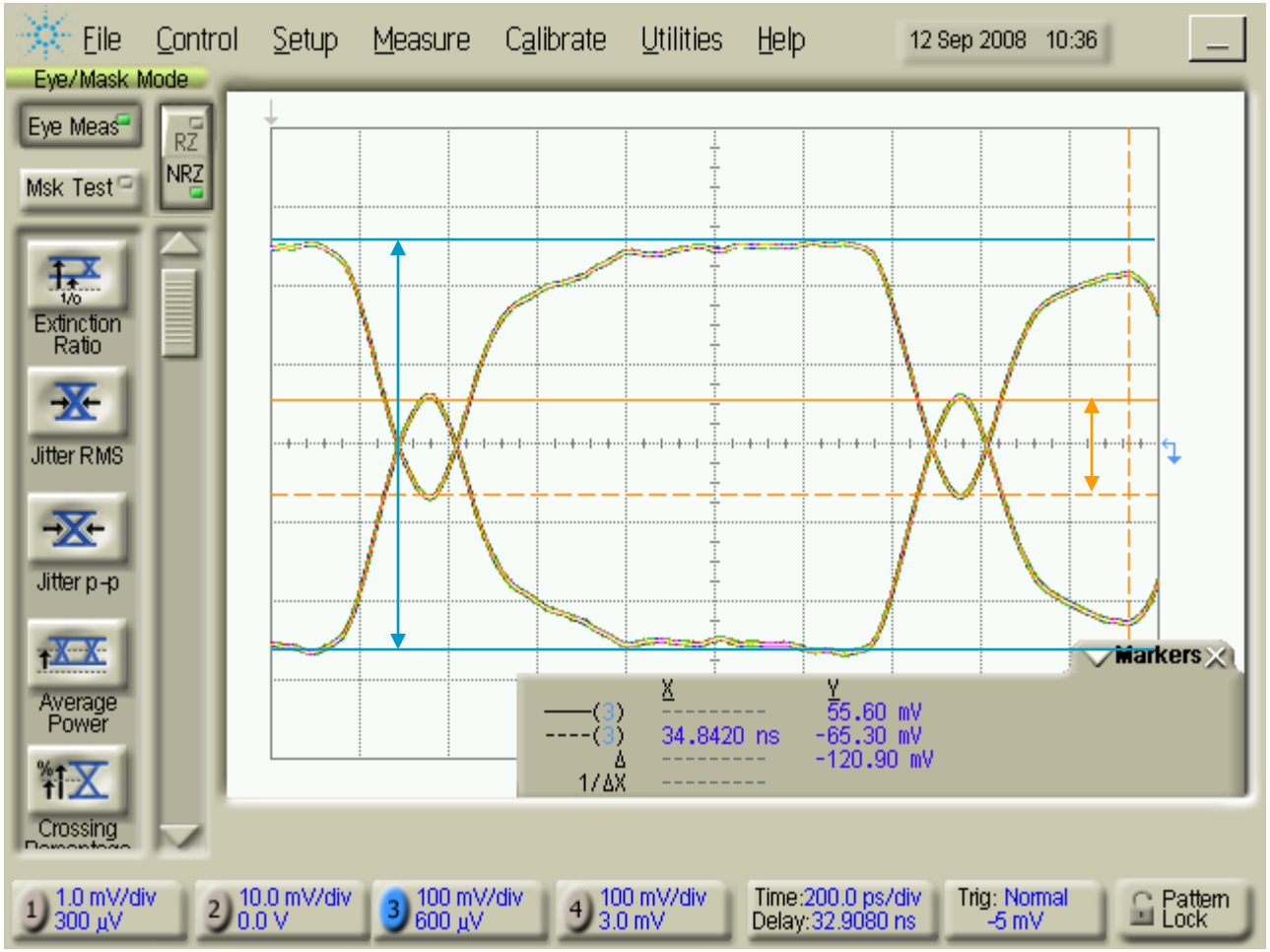
- channel is specified in terms of pulse amplitude compression[1], not directly in terms of ISI or DJ

  [1] there is a return loss spec of <20dB as well



- a total of DJ=88ps is specified
  - combined from ISI from channel (maybe less than 88ps) plus
  - swept PJ (1.5MHz...100MHz)

Trace # 2 OK for PCI Express 2.0

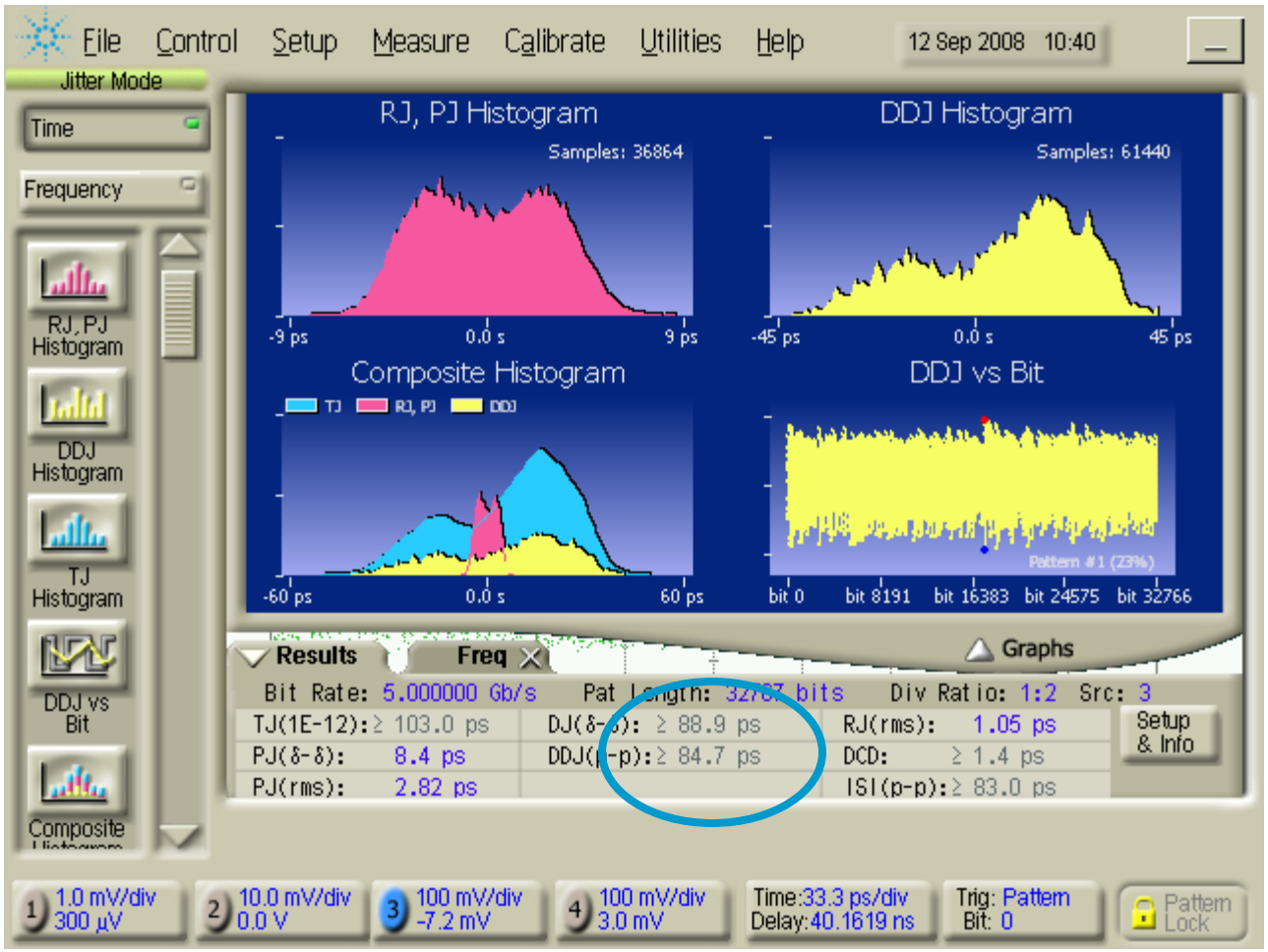


pattern:
1111 1011 1111 1111
0000 0100 0000 0000
normal only, trig / 16

levels of lone 1 (0) are about 20% of those of long duration.

Levels of long duration are equivalent to those of w/o channel

ISI “compliant channel” (trace # 2)



PRBS 2^{15}-1
through trace # 2
⇒84ps ISI
⇒add ~4ps PJ,100MHz
⇒DJ=88ps

Summary: RX tolerance Jitter Specs (Base Spec)

two different clocking architectures:

common ref-clk

- RX sampling on (multiplied) ref clk
- RX w /DLL only
- SSC off: no phase error induced
- SSC on:
  - small error (fempto seconds) due to path delay difference (!) but
  - significant residual phase error due to potentially different transfer functions (BW and peaking) of TX and RX clock multiplying PLLs

data clocked (embedded clock)

- RX w/ PLL-CDR (using ref clock only until locked)
- SSC on or off
  - common for TX and RX
  - both TX's use same ref clk

		Com Ref-clk				Data Clocked	
		rms	**pp**			**rms**	**pp**
SSC			residual: 75	**SSC**			20 ns
RJ (?)	HF	3.4	47.6	**RJ (?)**	HF	4.2	58.8
	LF	4.2	58.8		LF	8.0	112
RJ,sqrt sum		5.4	75.7	**RJ,sqrt sum**		9.0	126.5
DJ	HF		88	**DJ**	HF		88
					"UHF"		
total	sqrt		**150.7** - 238.7	**total**	sqrt		**126.5 - 214.5**

Summary: RX Tolerance Jitter Specs (Card Spec)

two different clocking architectures:

common ref-clk

- RX sampling on (multiplied) ref clk
- RX w /DLL only
- SSC off: no phase error induced
- SSC on:
  - small error (fempto seconds) due to path delay difference (!) but
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data clocked (embedded clock)

- RX w/ PLL-CDR (using ref clock only until locked)
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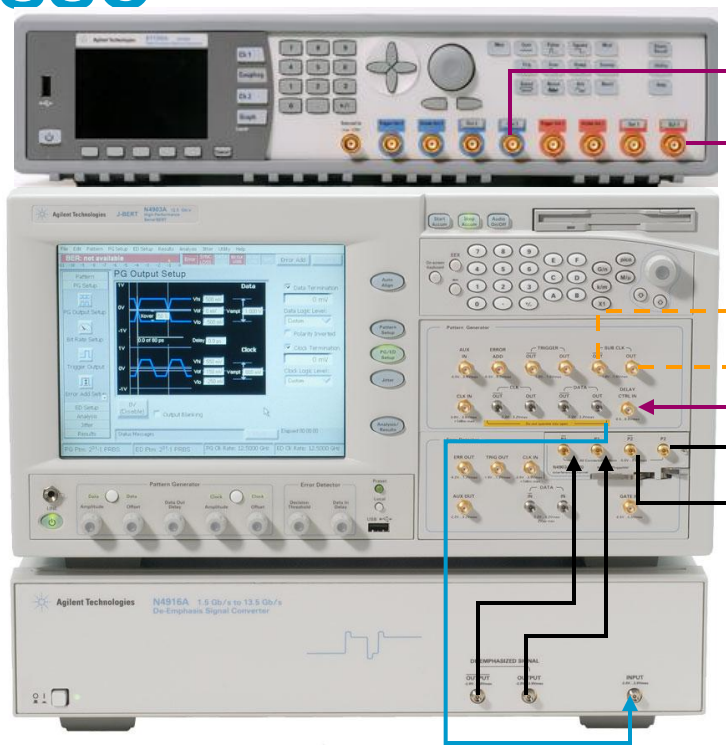
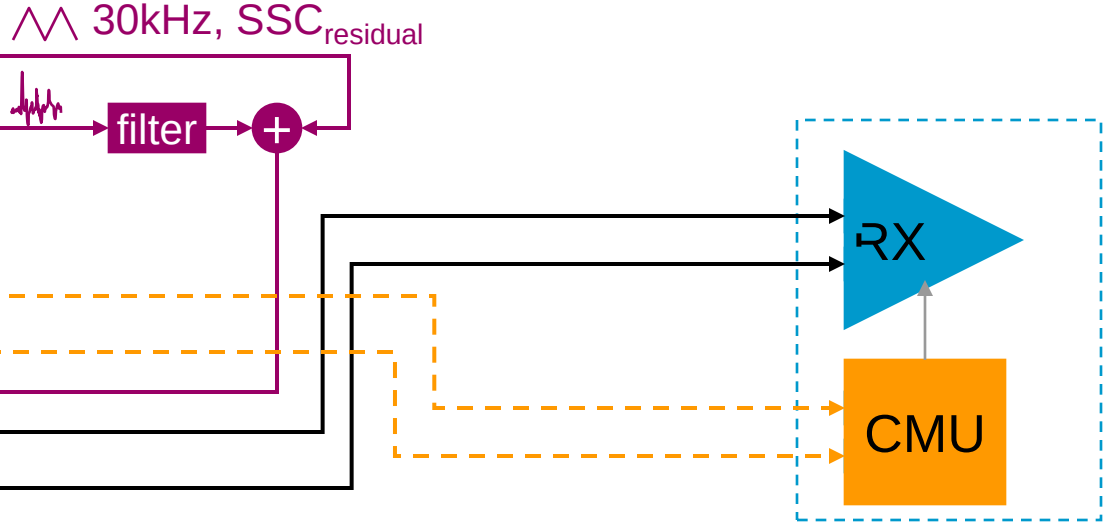
		Com Ref-clk				Data Clocked	
		rms	**pp**			**rms**	**pp**
SSC			residual: 75	**SSC**			20 ns
RJ (?)	HF	3.4	47.6	**RJ (?)**	HF	1.4	58.8
	LF	4.2	58.8		LF	3.0	112
RJ,sqrt sum		5.4	75.7	**RJ,sqrt sum**		9.0	126.5
DJ	HF		30	**DJ**	HF		30
	"UHF"		27		"UHF"		27
total	sqrt		132.7	**total**	sqrt		**126.5**

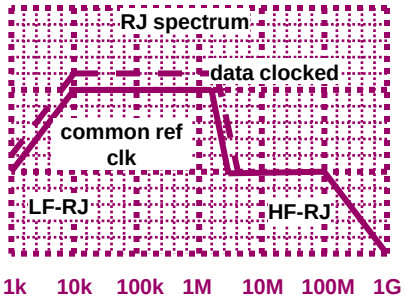
Three Steps To RX-jitter Tolerance Testing

1. Prepare DUT-RX for test
   - exit mission mode
   - enter test mode, set into loopback-mode
2. Stimulate DUT with all required signals and applicable properties
   - free running or synchronized to DUT
   - signal levels
   - delay between signals
   - jitter, absolute and between signals
3. Determine correctness of RX's conversion
   - synch on looped back data
   - analyze digital content: de-code, unpack, strip idles, …
   - compare and count errors: BER, FER,…

J-BERT, with 81150A for Spectral RJ and Residual SSC







- RJ generated through appropriately filtered noise from and external modulation capability of J-BERT
  residual SSC generated through 2nd Pulsar channel
- DJ (ISI+PJ) generated by J-BERT: trace #2 and internal source
- de-box used if de-emphasized signals are required
- patterns for DUT-RX programming available

Outlook PCIe-3

PCIe3, rev 0.5

- Symbol rate 8Gbs (includes a coding of 130/128?)
- some as PCIe2, **two architectures**, common ref clk and data clocked
  - **common ref clk**: BERT sources **clean clock** & **residual SSC** on **data**
  - **data clocked**: no clock supplied but **full SSC** on data
- RX measured **w/ & w/o ISI-channel** (calibration channel) - specs tbd
- **RJ** is always **spectrally flat** between 10MHz and 1GHz
- **PJ** is **two-tone sinusoidal** (two frequencies **simultaneously**!)
  - 1st tone 70ps if 10KHz-1MHz, or 70..7ps if 1MHz-10MHz (tbd)
  - 2nd tone 7ps, 10MHz-1GHz (tbd)
- Noise injection
  - common mode: single sinusoidal; Vpp and frq tbd
  - differential mode: spectrally flat white noise BW (>1GHz), Vpp tbd
- DCD 4ps
- necessity of de-emph tbd in rev .07